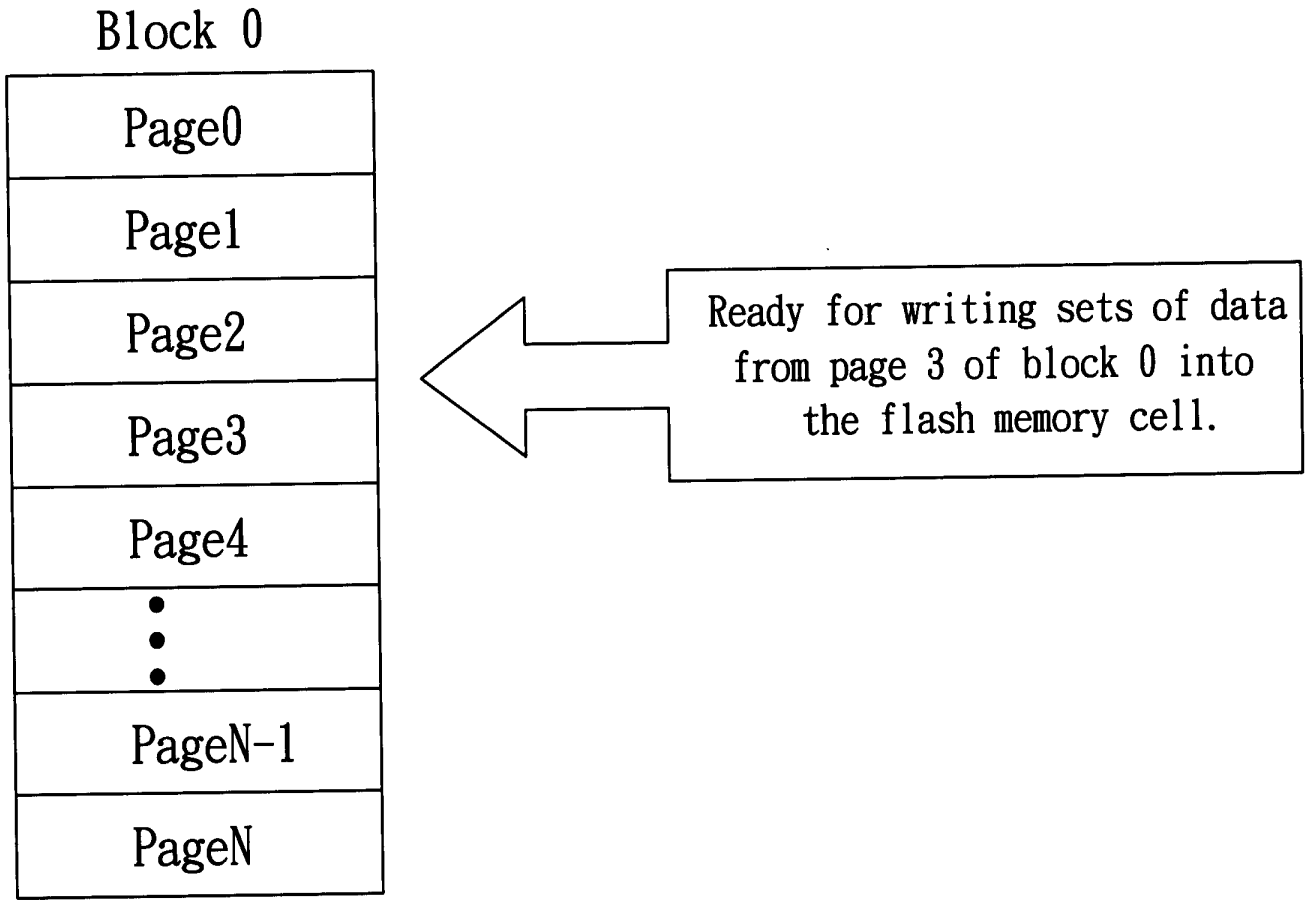
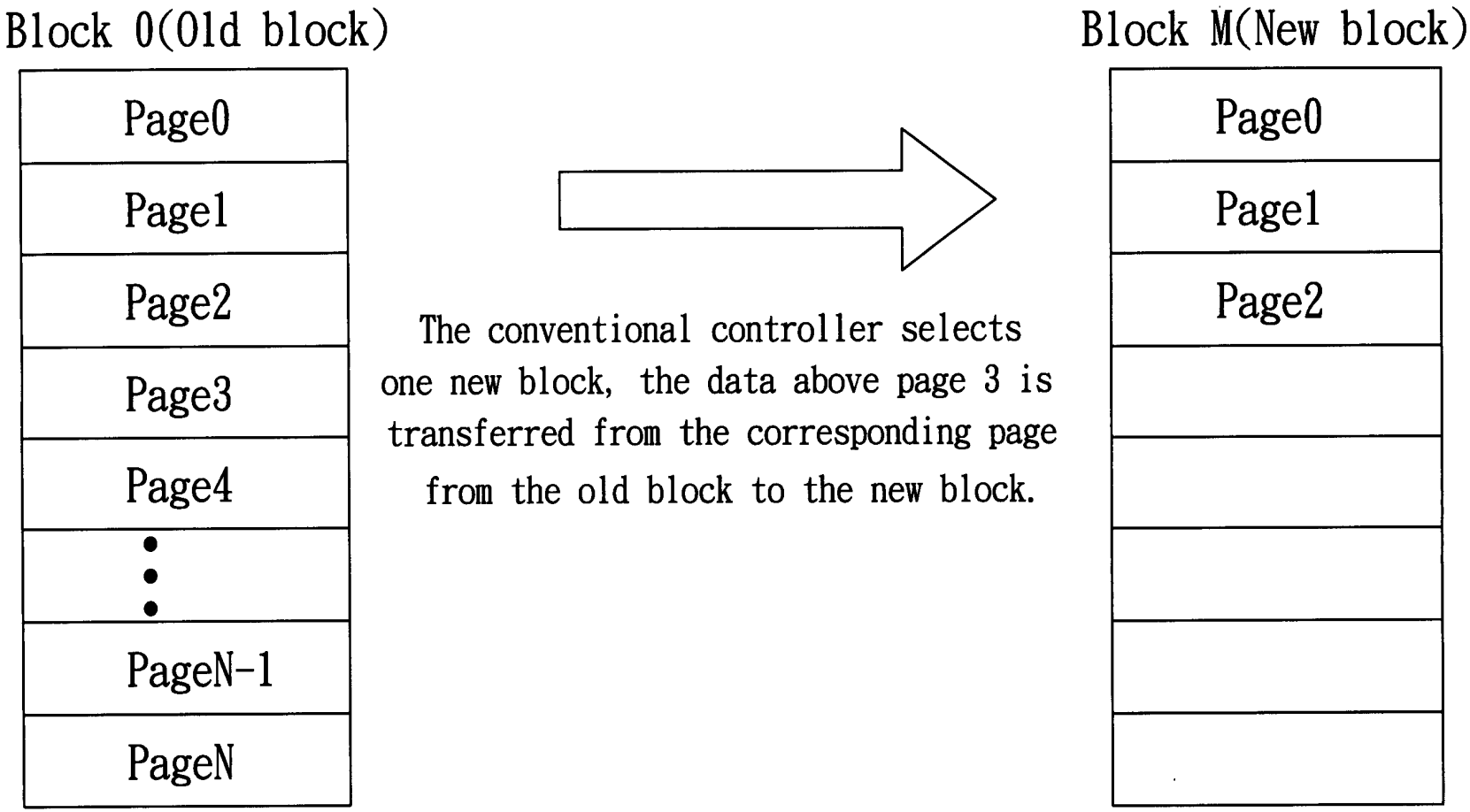
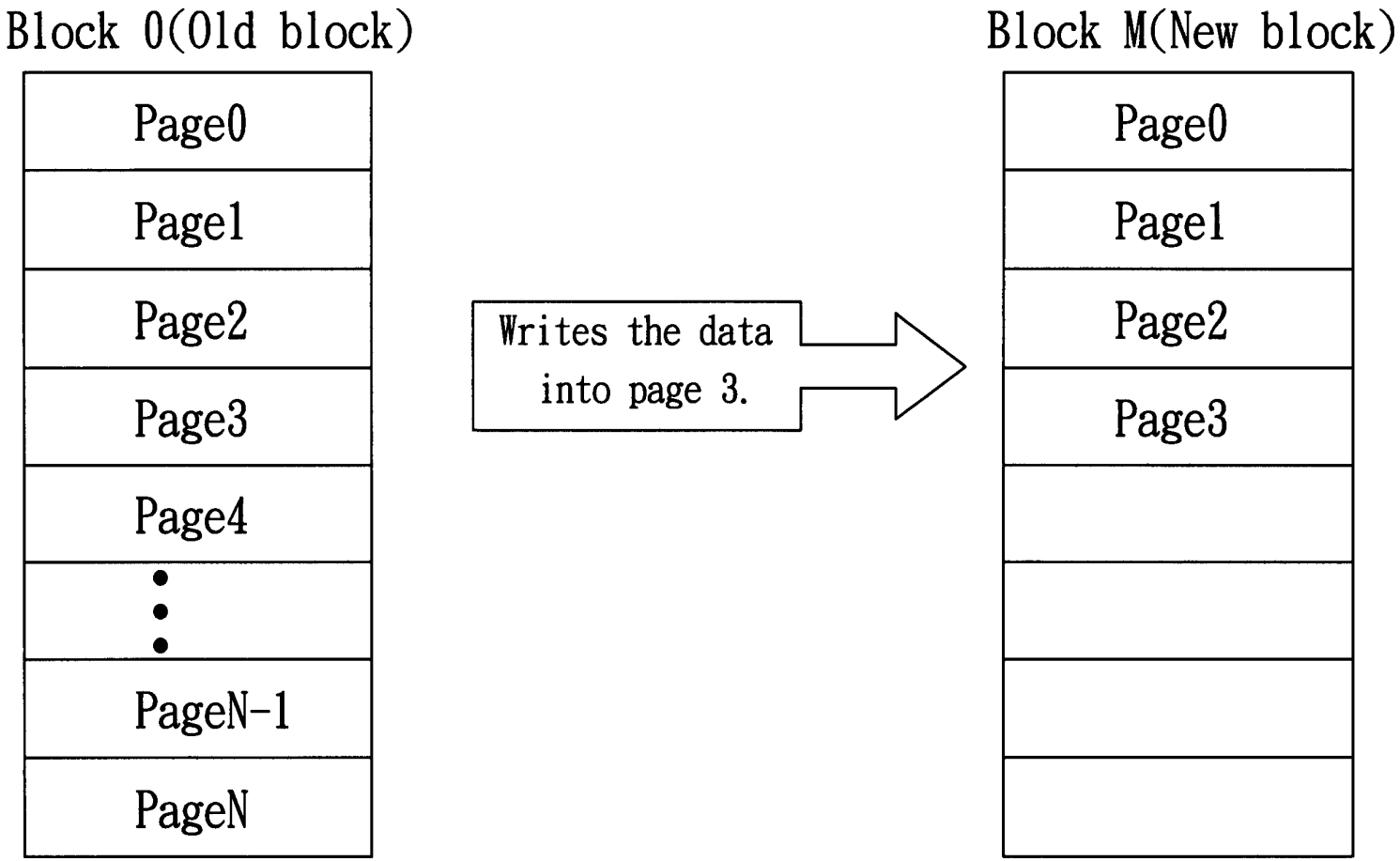


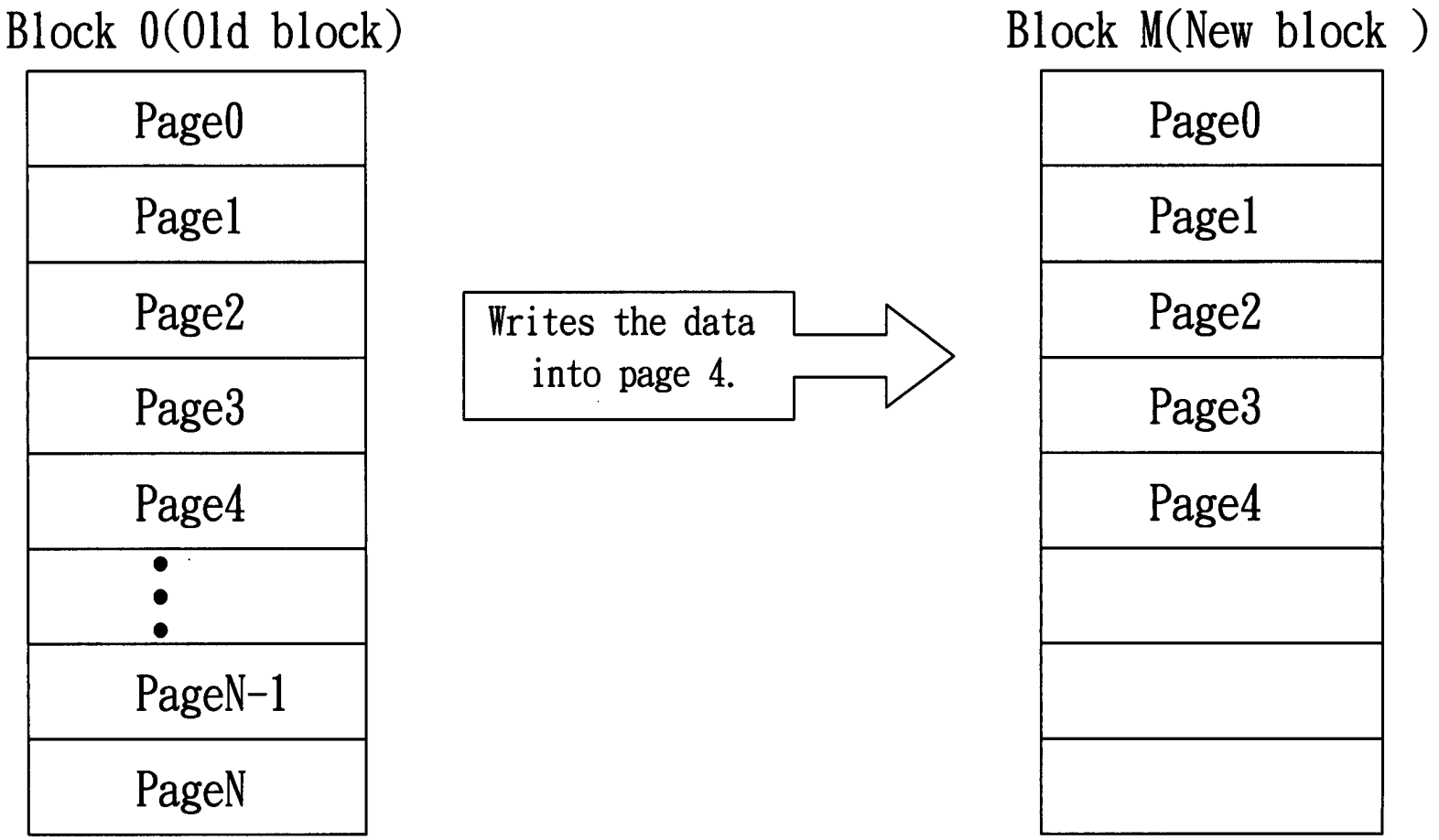
PRIOR ART
FIG. 1A



PRIOR ART
FIG.1B

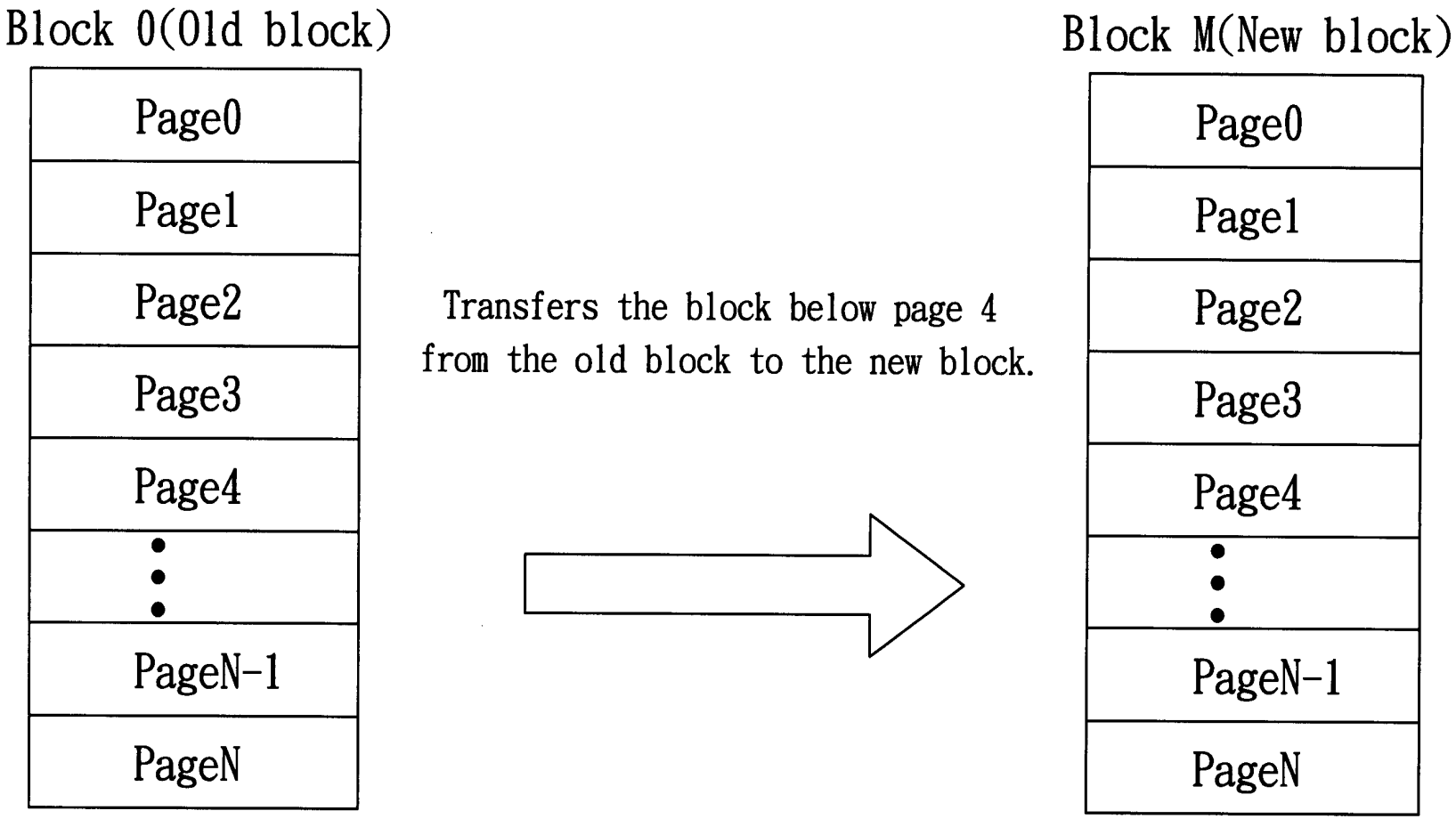


PRIOR ART
FIG.1C

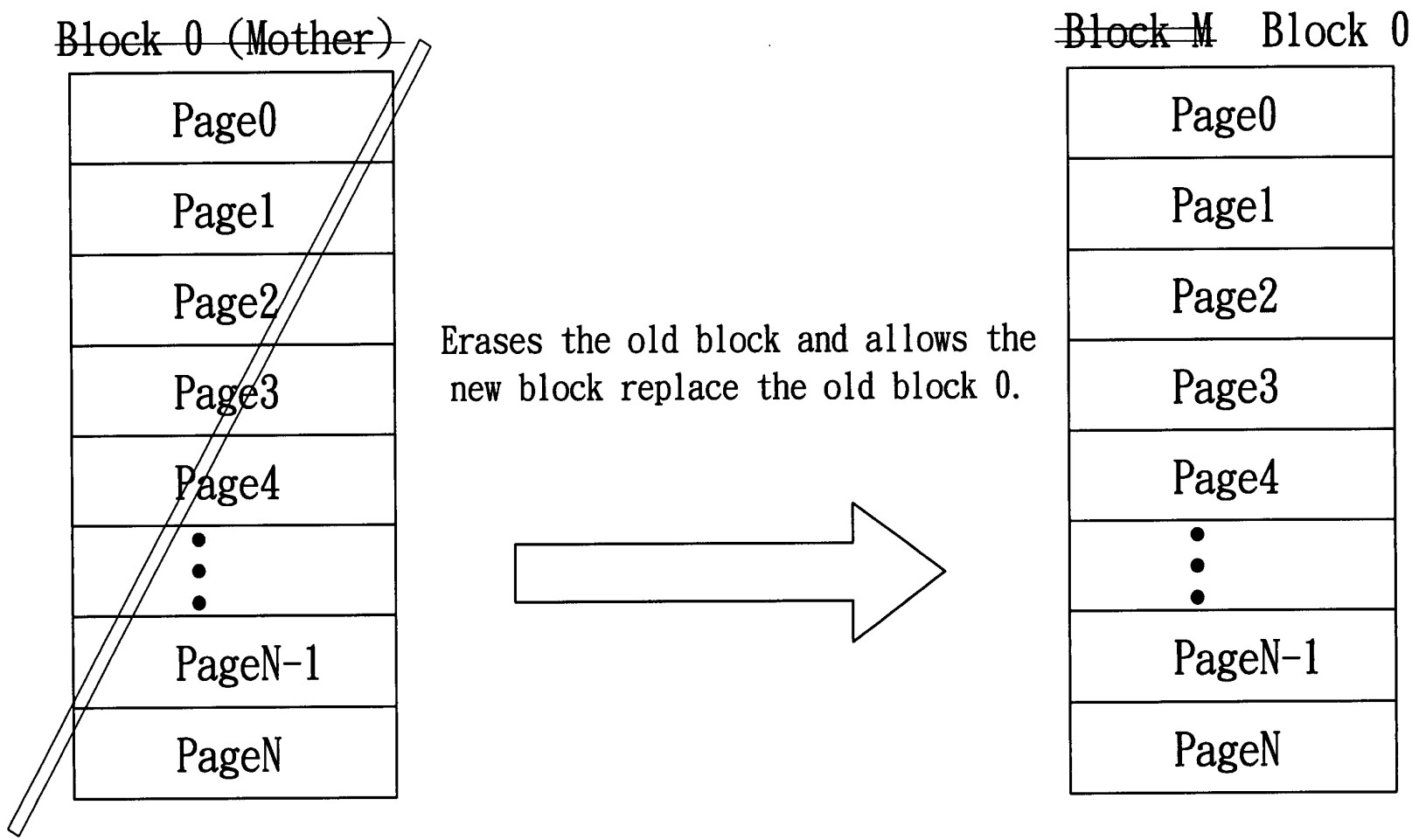


PRIOR ART

FIG. 1D



PRIOR ART
FIG.1E



PRIOR ART
FIG.1F

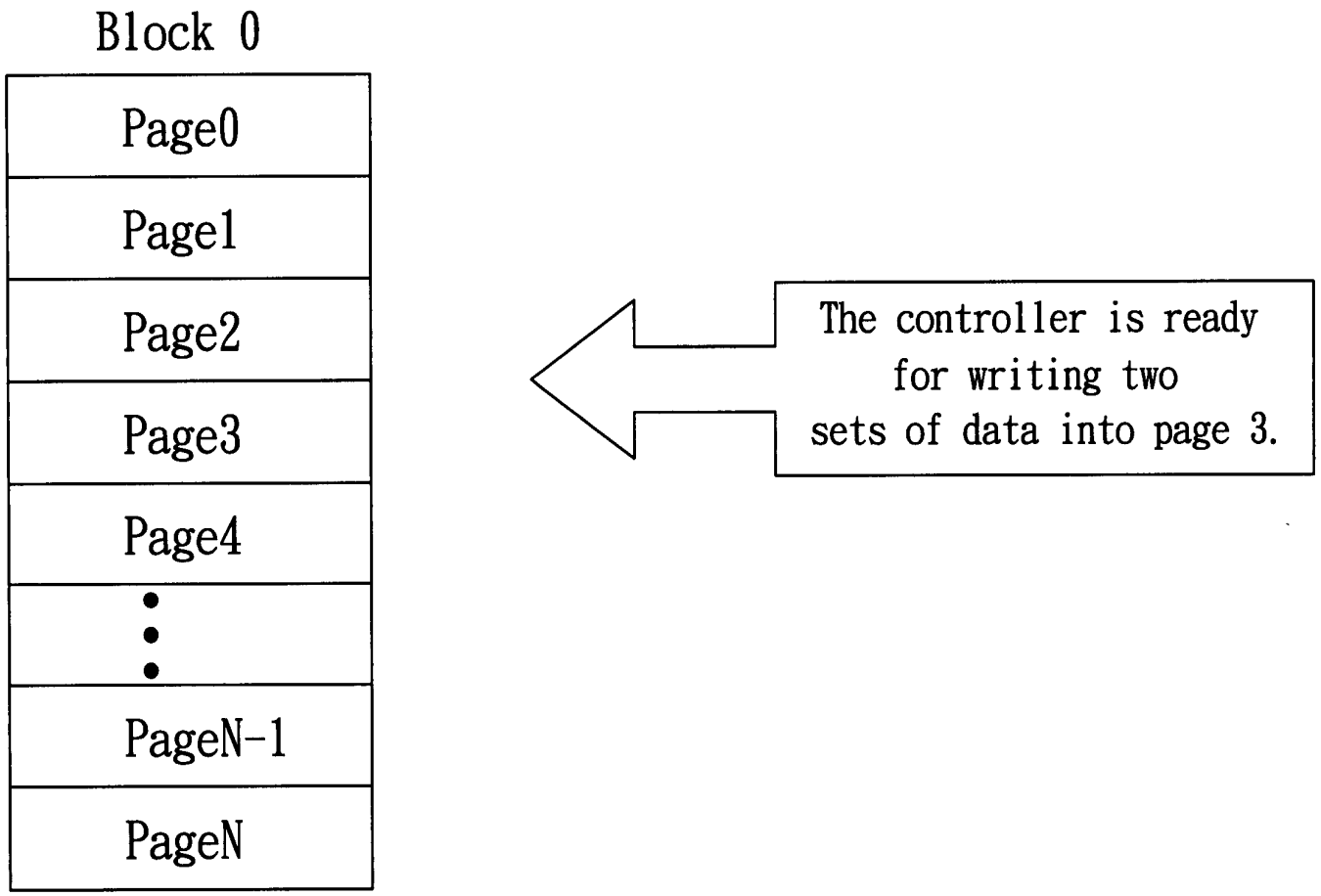

Block 0
Page0
Page1
Page2
Page3
Page4
PageN-1
PageN
The controller is ready for writing two sets of data into page 3.

FIG.2A

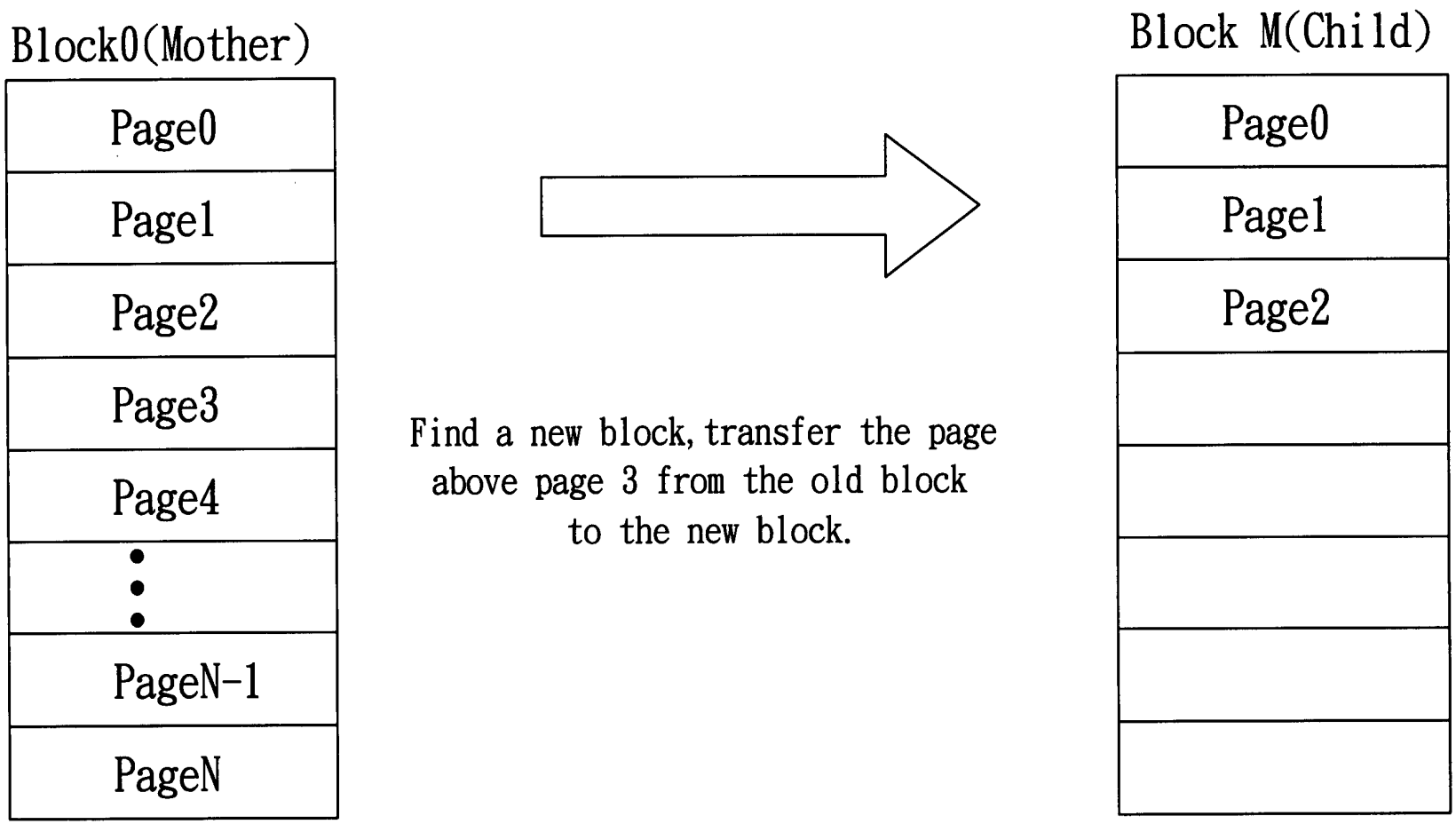

Block0(Mother)
Page0
Page1
Page2
Page3
Page4
PageN-1
PageN
Find a new block, transfer the page above page 3 from the old block to the new block.
Block M(Child)
Page0
Page1
Page2

FIG.2B

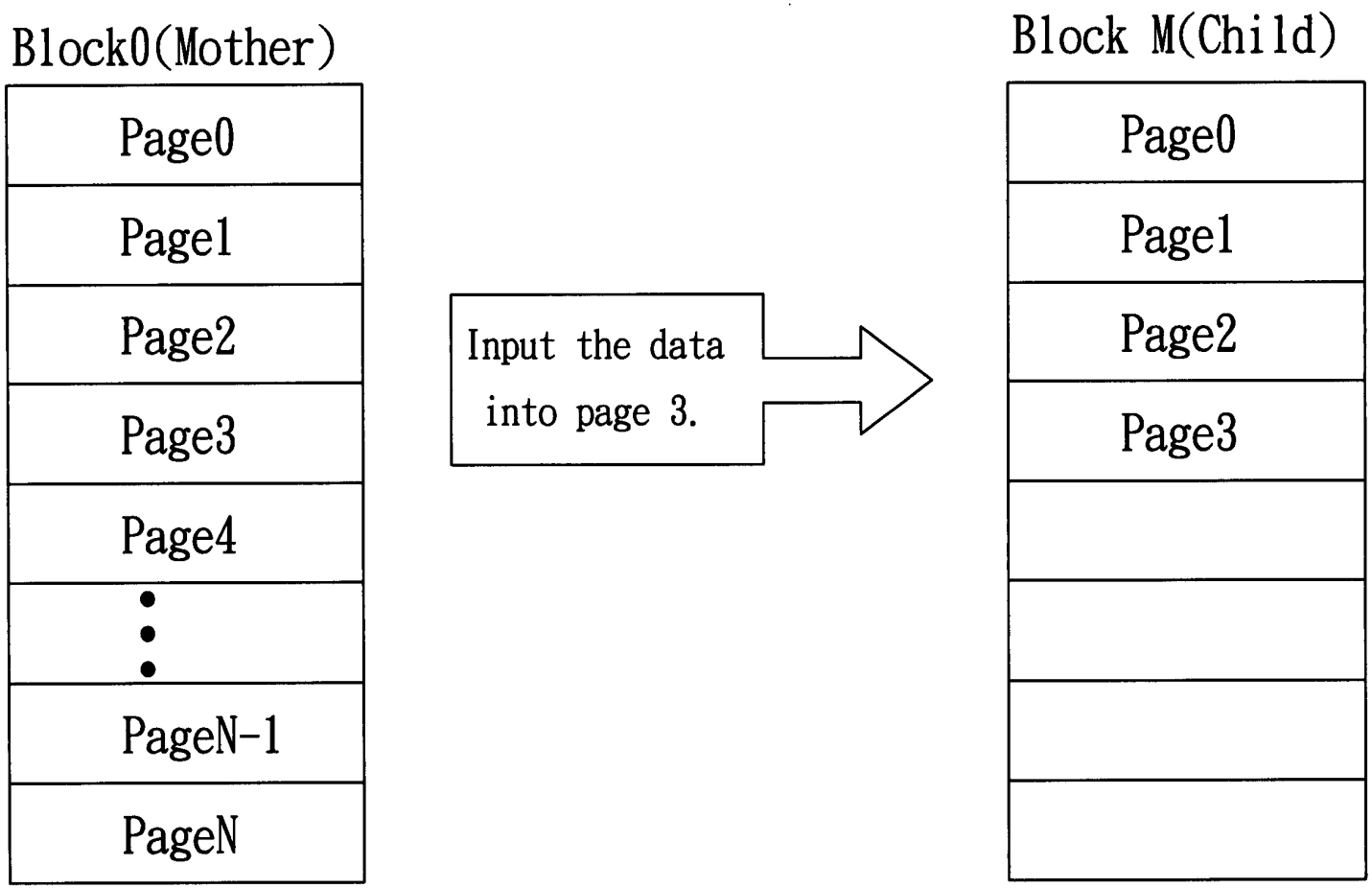

Block0(Mother)
Page0
Page1
Page2
Page3
Page4
PageN-1
PageN
Input the data into page 3.
Block M(Child)
Page0
Page1
Page2
Page3

FIG.2C

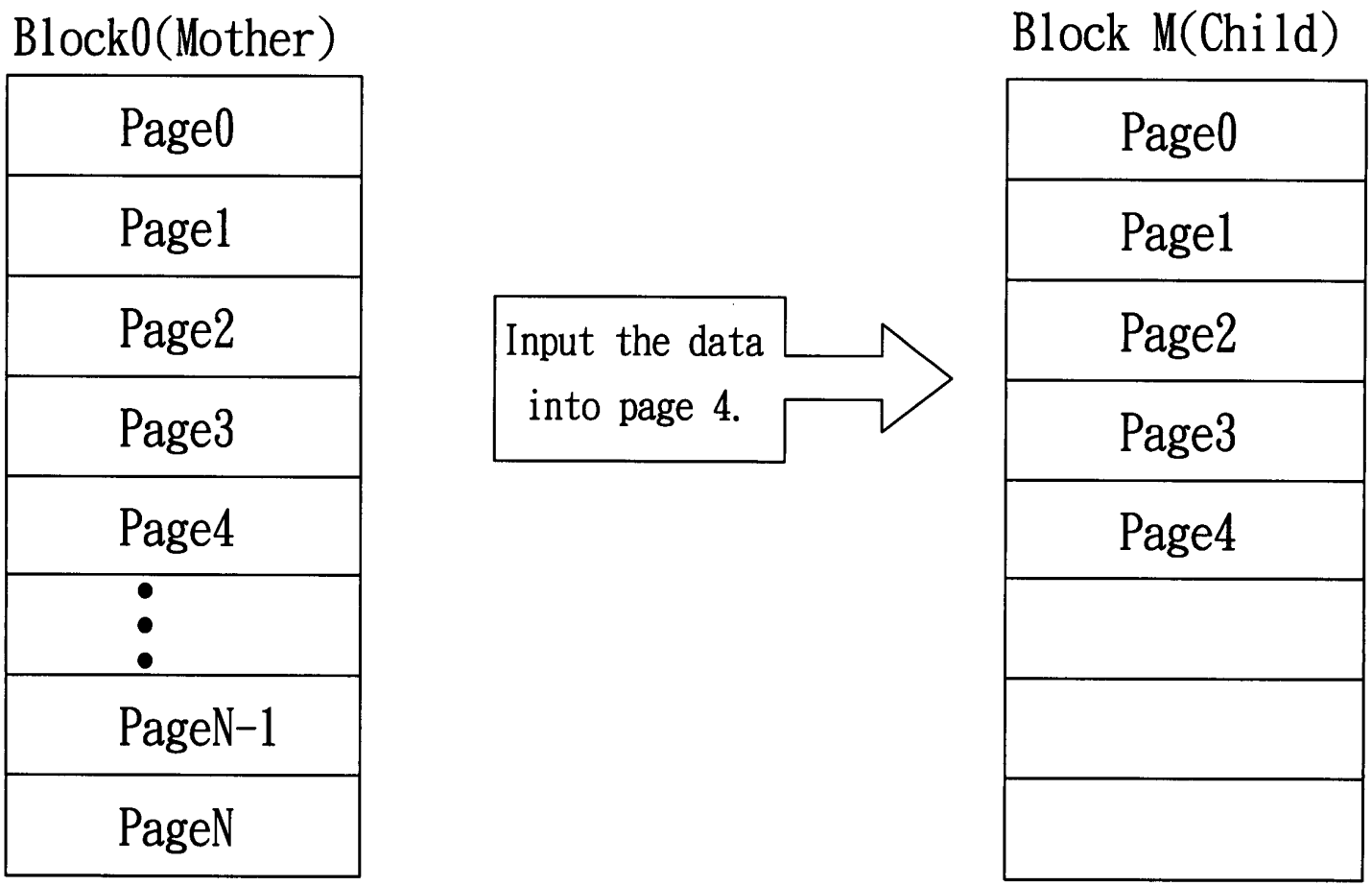

Block0(Mother)
Page0
Page1
Page2
Page3
Page4
PageN-1
PageN
Input the data into page 4.
Block M(Child)
Page0
Page1
Page2
Page3
Page4

FIG.2D

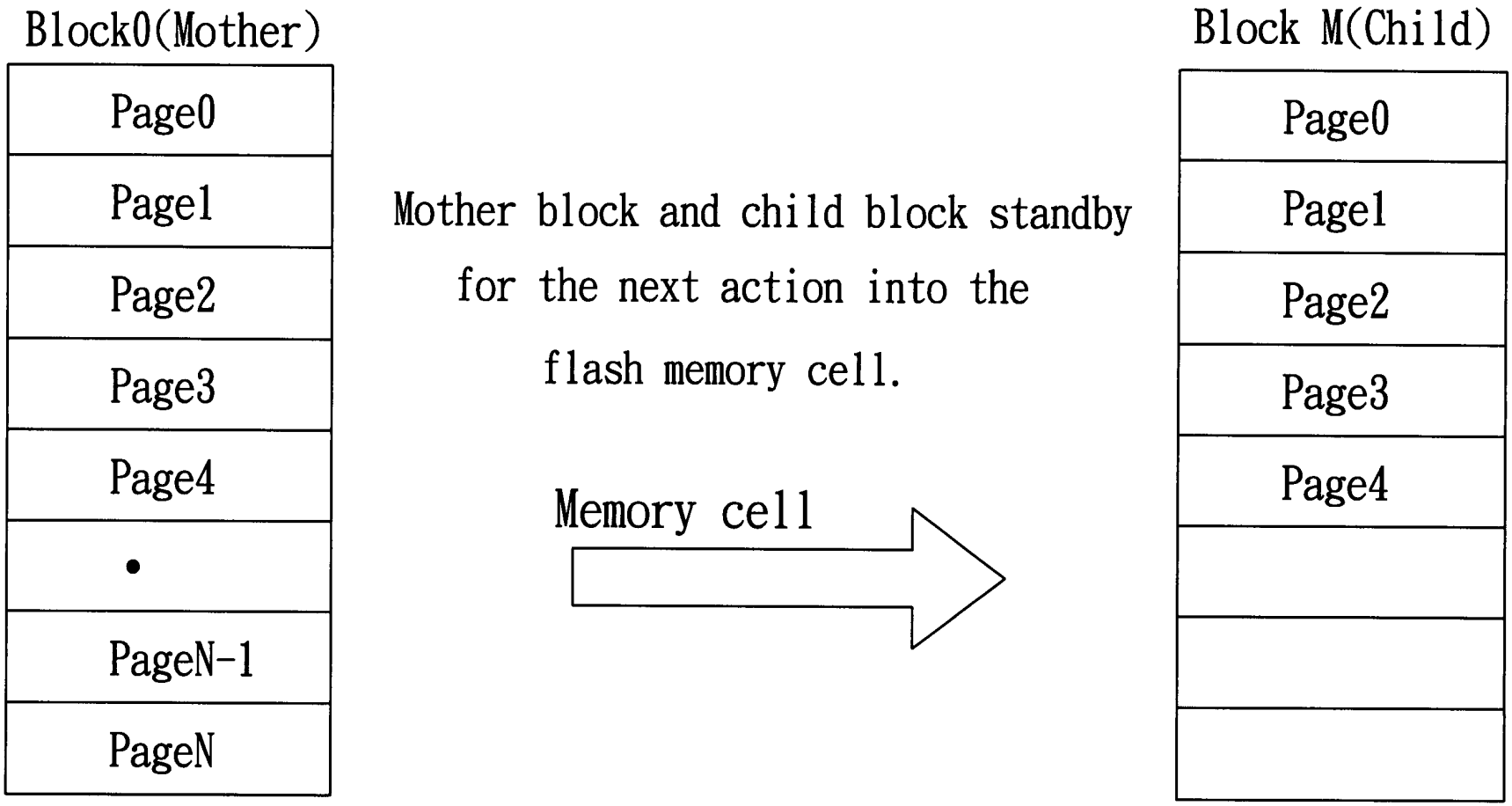

Block0(Mother)
Page0
Page1
Page2
Page3
Page4
•
PageN-1
PageN
Mother block and child block standby for the next action into the flash memory cell.
Memory cell
Block M(Child)
Page0
Page1
Page2
Page3
Page4

FIG.2E

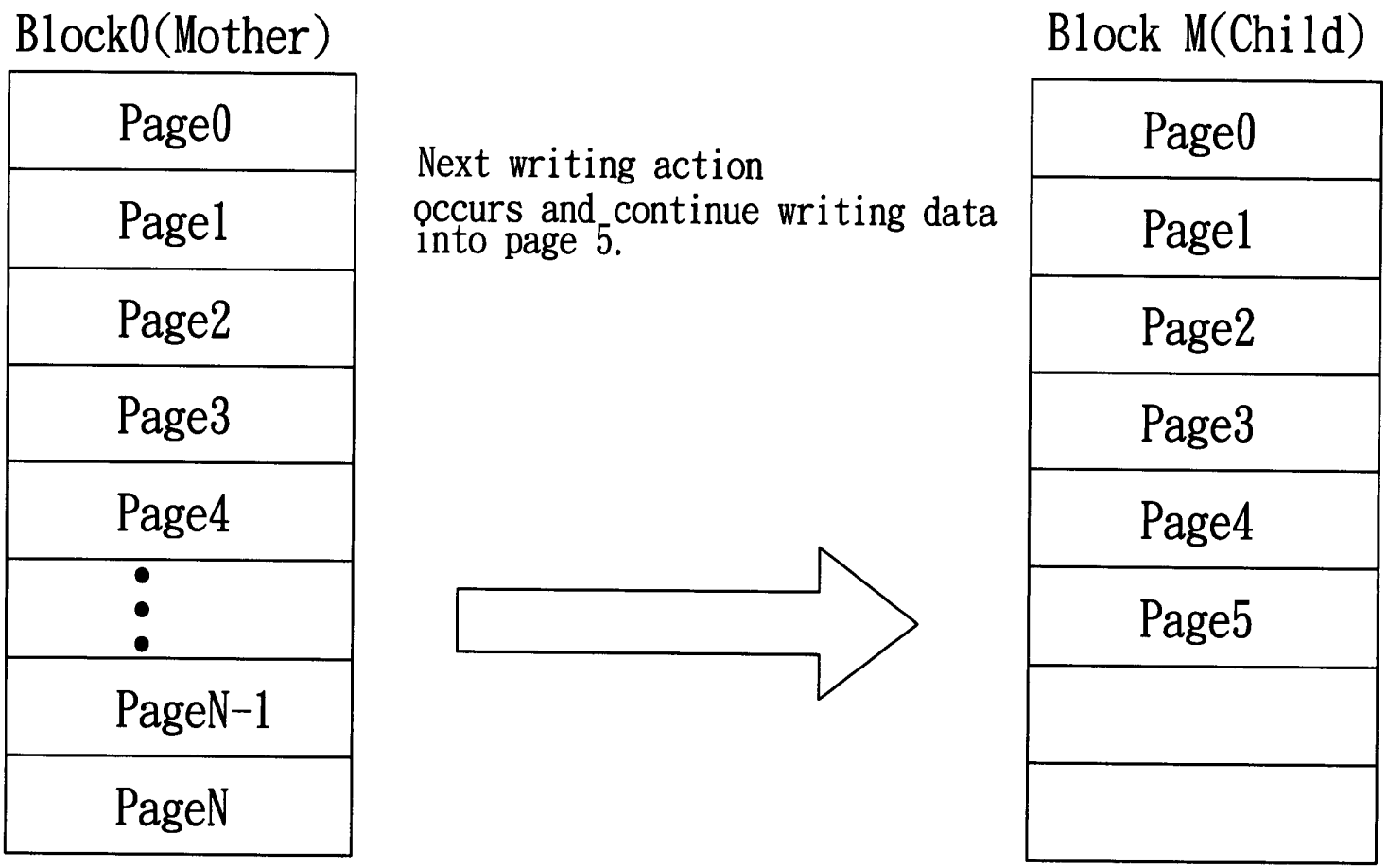

Block0(Mother)
Page0
Page1
Page2
Page3
Page4
PageN-1
PageN
Next writing action
occurs and continue writing data
into page 5.
Block M(Child)
Page0
Page1
Page2
Page3
Page4
Page5

FIG.2F

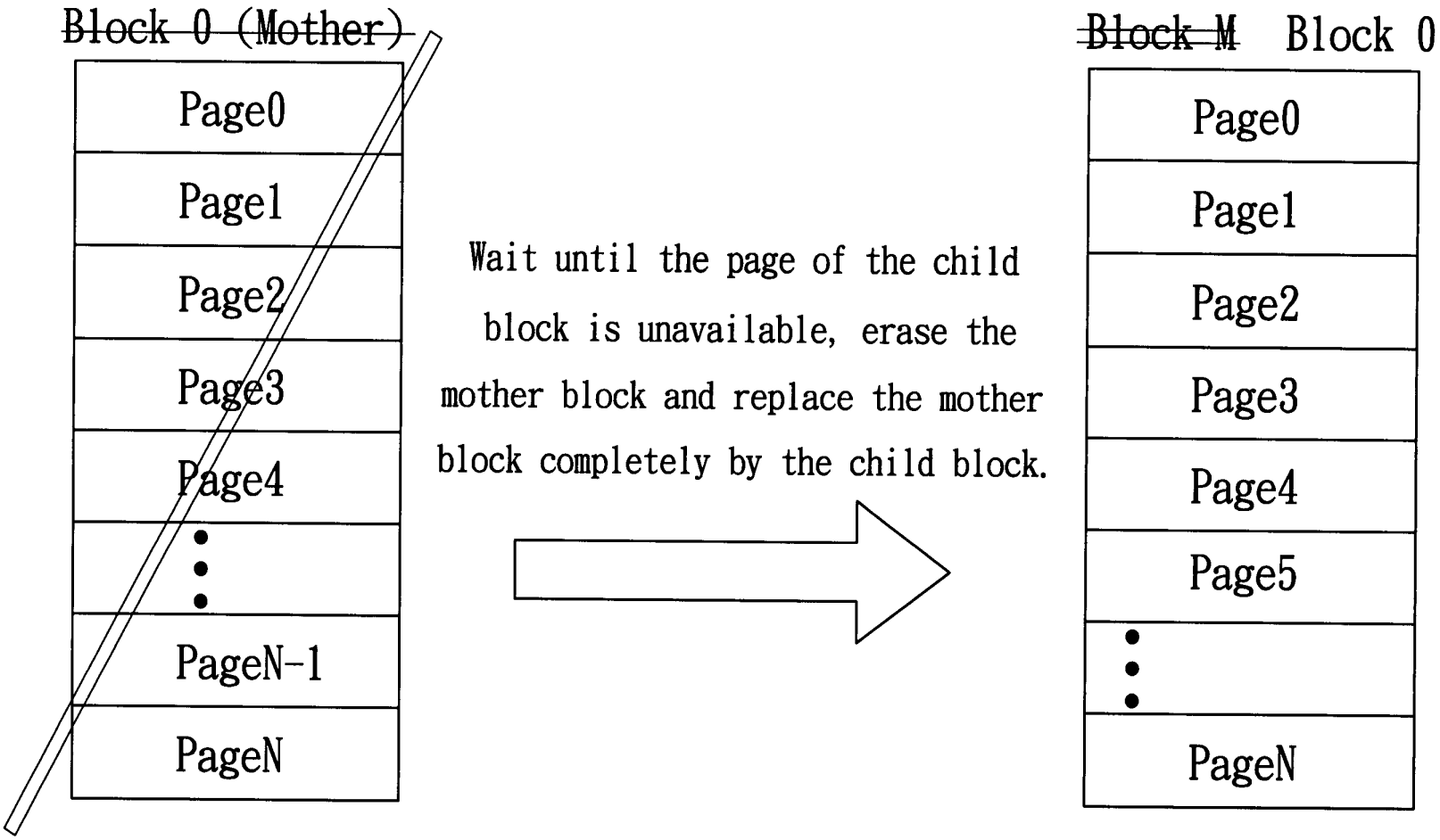

Block 0 (Mother)
Page0
Page1
Page2
Page3
Page4
PageN-1
PageN
Wait until the page of the child block is unavailable, erase the mother block and replace the mother block completely by the child block.
Block M
Block 0
Page0
Page1
Page2
Page3
Page4
Page5
PageN

FIG.2G

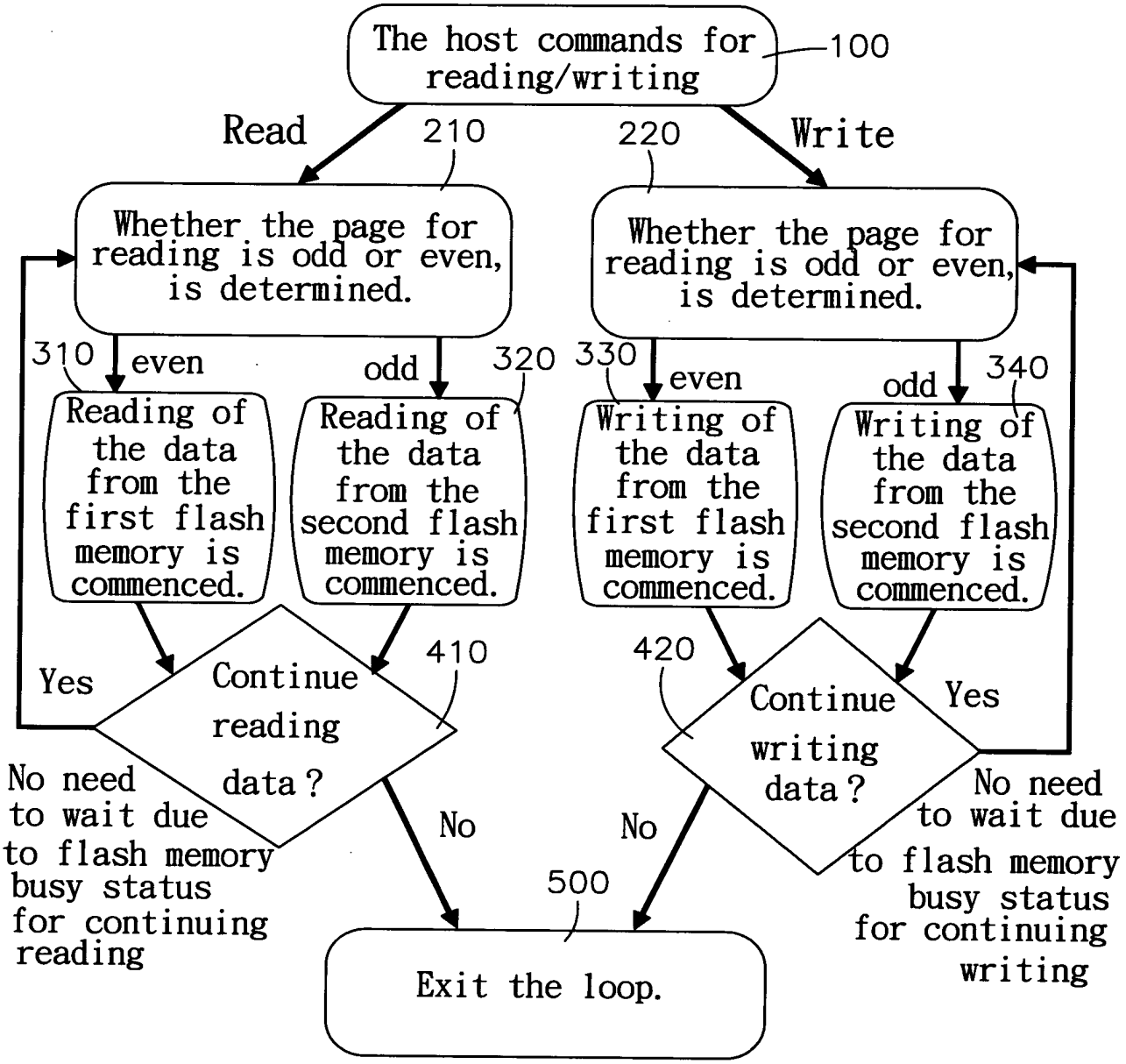

The host commands for reading/writing
100
Read
210
220
Write
Whether the page for reading is odd or even, is determined.
Whether the page for reading is odd or even, is determined.
310
even
odd
320
330
even
odd
340
Reading of the data from the first flash memory is commenced.
Reading of the data from the second flash memory is commenced.
Writing of the data from the first flash memory is commenced.
Writing of the data from the second flash memory is commenced.
410
420
Yes
Continue reading data ?
Continue writing data ?
Yes
No need to wait due to flash memory busy status for continuing reading
No
No
No need to wait due to flash memory busy status for continuing writing
500
Exit the loop.

FIG.3

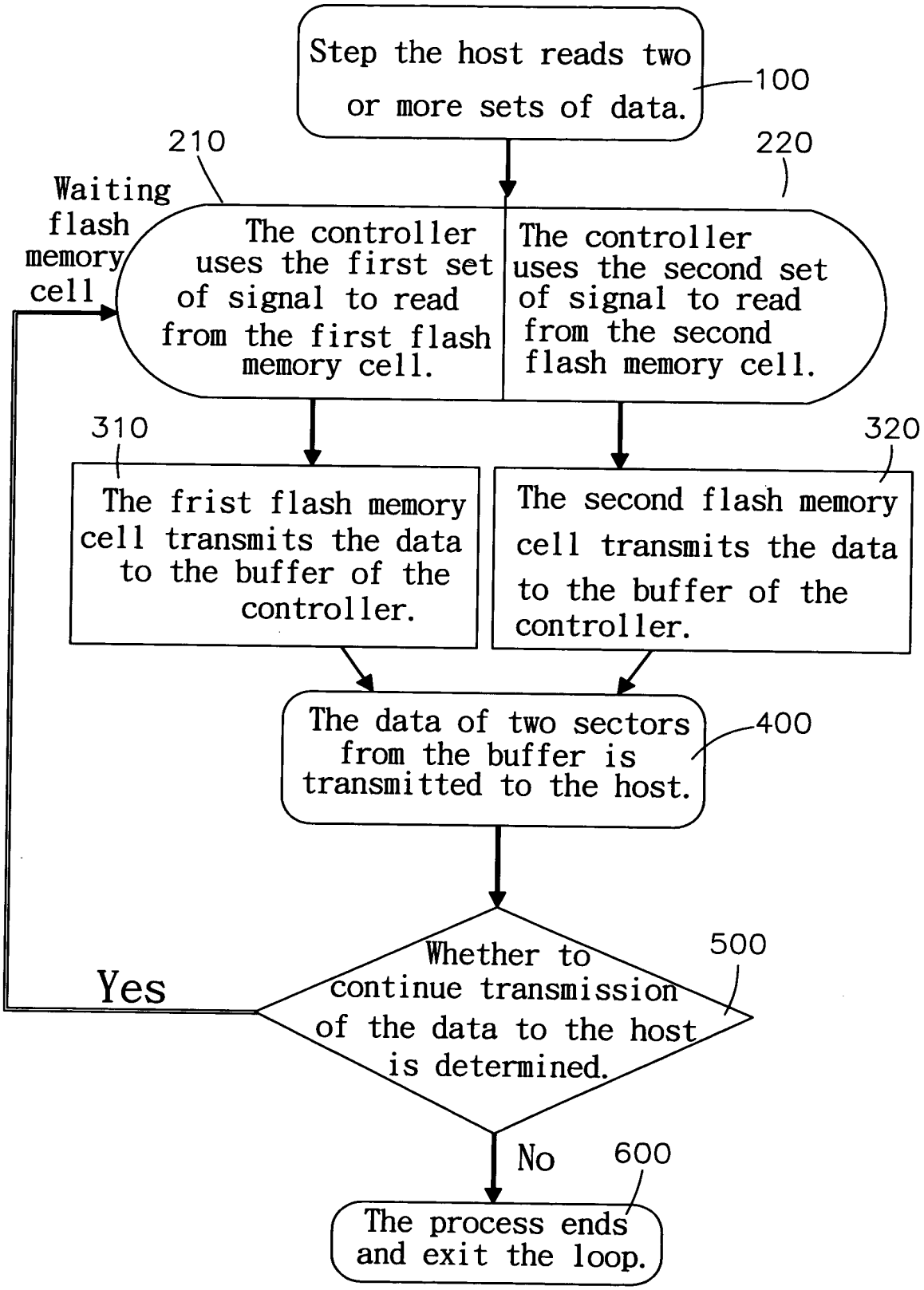

Step the host reads two or more sets of data.
100
210
220
Waiting flash memory cell
The controller uses the first set of signal to read from the first flash memory cell.
The controller uses the second set of signal to read from the second flash memory cell.
310
320
The frist flash memory cell transmits the data to the buffer of the controller.
The second flash memory cell transmits the data to the buffer of the controller.
The data of two sectors from the buffer is transmitted to the host.
400
Whether to continue transmission of the data to the host is determined.
500
Yes
No
600
The process ends and exit the loop.

FIG. 4A

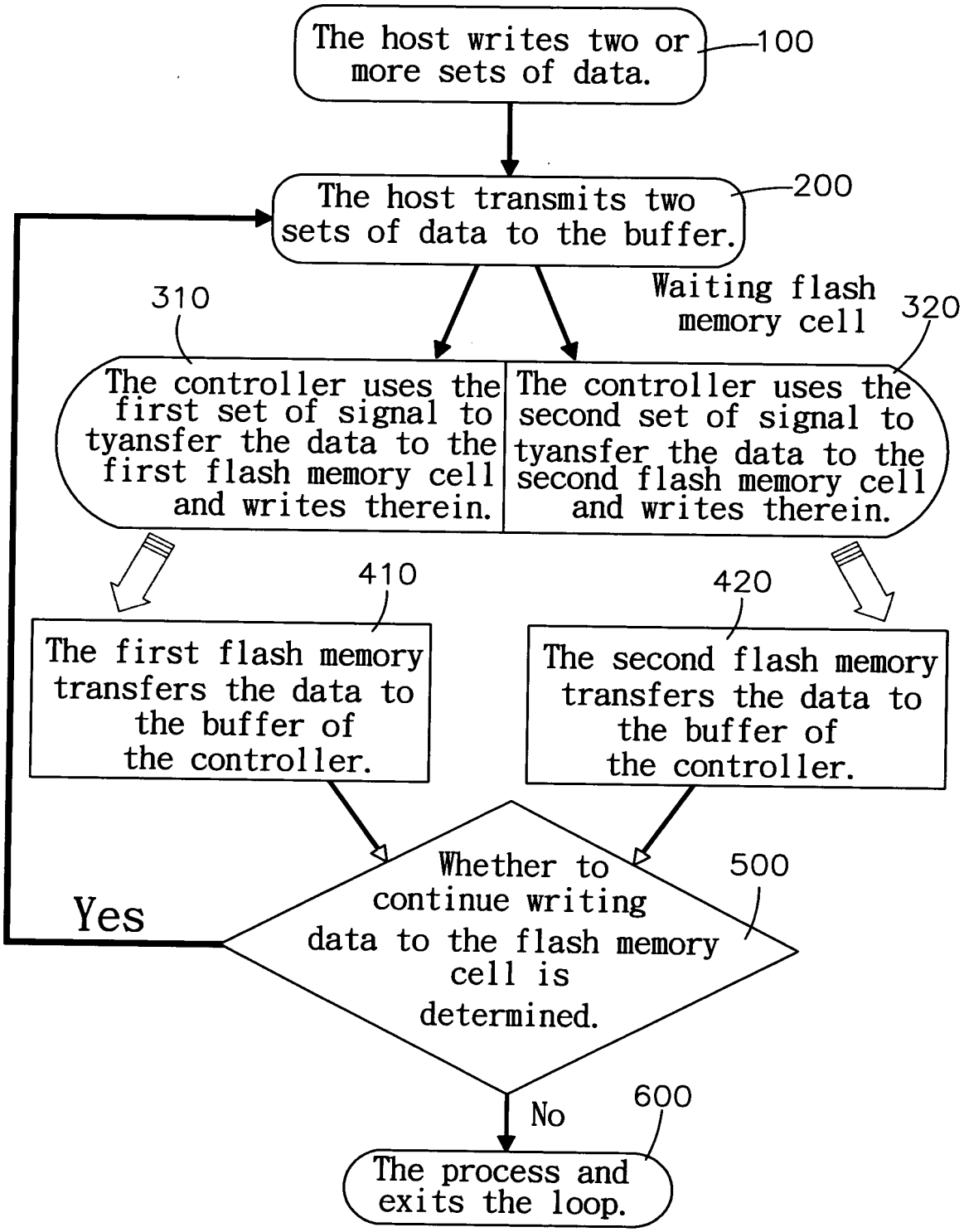

The host writes two or more sets of data.
100
The host transmits two sets of data to the buffer.
200
310
Waiting flash memory cell
320
The controller uses the first set of signal to tyansfer the data to the first flash memory cell and writes therein.
The controller uses the second set of signal to tyansfer the data to the second flash memory cell and writes therein.
410
420
The first flash memory transfers the data to the buffer of the controller.
The second flash memory transfers the data to the buffer of the controller.
Whether to continue writing data to the flash memory cell is determined.
500
Yes
No
600
The process and exits the loop.

FIG. 4B

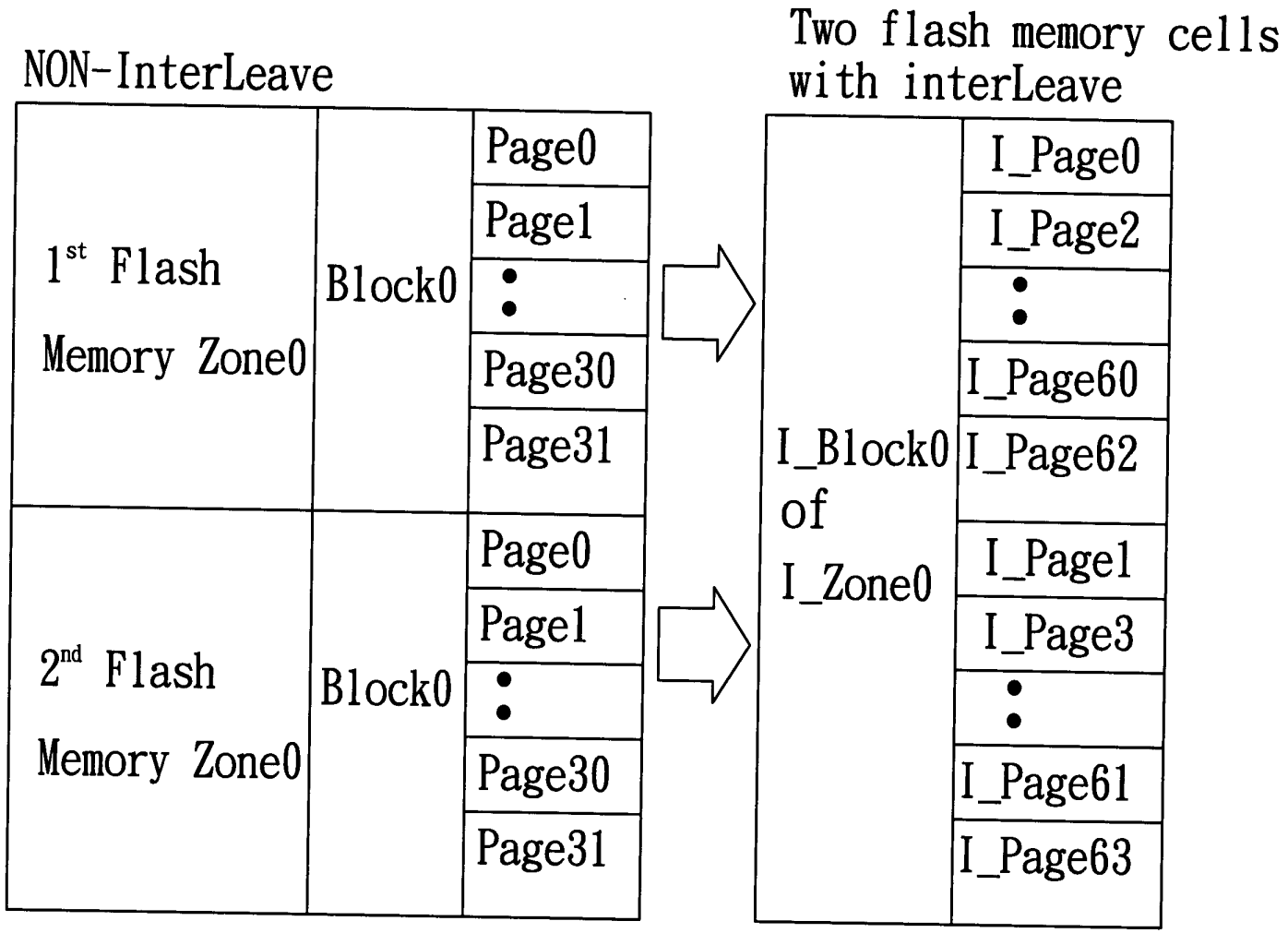

NON-InterLeave
1st Flash Memory Zone0
Block0
Page0
Page1
Page30
Page31
2nd Flash Memory Zone0
Block0
Page0
Page1
Page30
Page31
Two flash memory cells with interLeave
I_Block0 of I_Zone0
I_Page0
I_Page2
I_Page60
I_Page62
I_Page1
I_Page3
I_Page61
I_Page63

FIG.5A

I_Zone0	I_Zone1	I_Zone2	I_Zone3
I_Block0	I_Block0	I_Block0	I_Block0
I_Block1	I_Block1	I_Block1	I_Block1
I_Block2	I_Block2	I_Block2	I_Block2
I_Block3	I_Block3	I_Block3	I_Block3
I_Block4	I_Block4	I_Block4	I_Block4
I_Block5	I_Block5	I_Block5	I_Block5
I_Block6	I_Block6	I_Block6	I_Block6
I_Block7	I_Block7	I_Block7	I_Block7
⋮	⋮	⋮	⋮
I_Block1016	I_Block1016	I_Block1016	I_Block1016
I_Block1017	I_Block1017	I_Block1017	I_Block1017
I_Block1018	I_Block1018	I_Block1018	I_Block1018
I_Block1019	I_Block1019	I_Block1019	I_Block1019
I_Block1020	I_Block1020	I_Block1020	I_Block1020
I_Block1021	I_Block1021	I_Block1021	I_Block1021
I_Block1022	I_Block1022	I_Block1022	I_Block1022
I_Block1023	I_Block1023	I_Block1023	I_Block1023

FIG. 5B

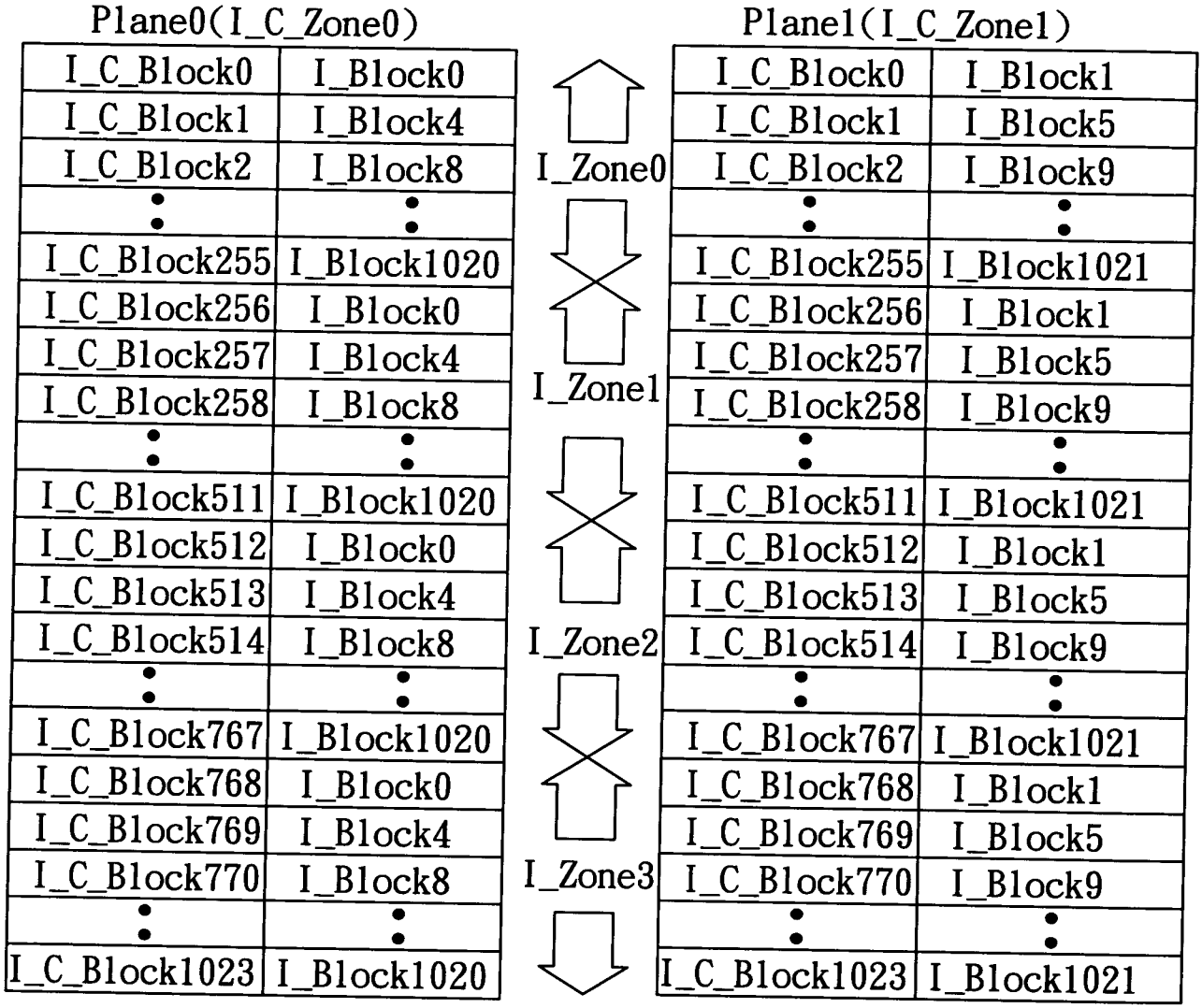

Plane0(I_C_Zone0)
I_C_Block0
I_Block0
I_C_Block1
I_Block4
I_C_Block2
I_Block8
I_C_Block255
I_Block1020
I_C_Block256
I_Block0
I_C_Block257
I_Block4
I_C_Block258
I_Block8
I_C_Block511
I_Block1020
I_C_Block512
I_Block0
I_C_Block513
I_Block4
I_C_Block514
I_Block8
I_C_Block767
I_Block1020
I_C_Block768
I_Block0
I_C_Block769
I_Block4
I_C_Block770
I_Block8
I_C_Block1023
I_Block1020
I_Zone0
I_Zone1
I_Zone2
I_Zone3
Plane1(I_C_Zone1)
I_C_Block0
I_Block1
I_C_Block1
I_Block5
I_C_Block2
I_Block9
I_C_Block255
I_Block1021
I_C_Block256
I_Block1
I_C_Block257
I_Block5
I_C_Block258
I_Block9
I_C_Block511
I_Block1021
I_C_Block512
I_Block1
I_C_Block513
I_Block5
I_C_Block514
I_Block9
I_C_Block767
I_Block1021
I_C_Block768
I_Block1
I_C_Block769
I_Block5
I_C_Block770
I_Block9
I_C_Block1023
I_Block1021

FIG. 6A

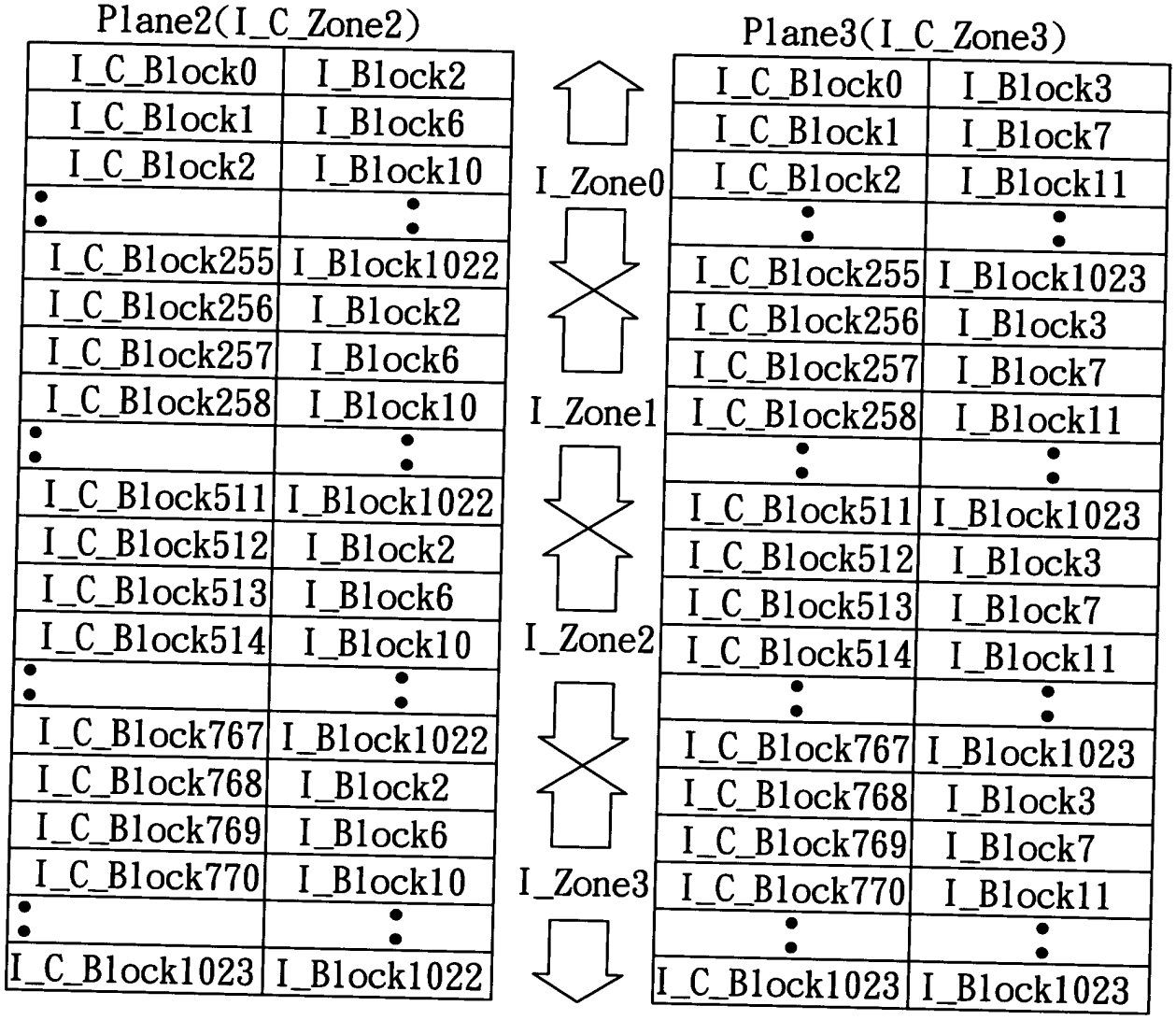

Plane2(I_C_Zone2)
I_C_Block0
I_Block2
I_C_Block1
I_Block6
I_C_Block2
I_Block10
I_C_Block255
I_Block1022
I_C_Block256
I_Block2
I_C_Block257
I_Block6
I_C_Block258
I_Block10
I_C_Block511
I_Block1022
I_C_Block512
I_Block2
I_C_Block513
I_Block6
I_C_Block514
I_Block10
I_C_Block767
I_Block1022
I_C_Block768
I_Block2
I_C_Block769
I_Block6
I_C_Block770
I_Block10
I_C_Block1023
I_Block1022
I_Zone0
I_Zone1
I_Zone2
I_Zone3
Plane3(I_C_Zone3)
I_C_Block0
I_Block3
I_C_Block1
I_Block7
I_C_Block2
I_Block11
I_C_Block255
I_Block1023
I_C_Block256
I_Block3
I_C_Block257
I_Block7
I_C_Block258
I_Block11
I_C_Block511
I_Block1023
I_C_Block512
I_Block3
I_C_Block513
I_Block7
I_C_Block514
I_Block11
I_C_Block767
I_Block1023
I_C_Block768
I_Block3
I_C_Block769
I_Block7
I_C_Block770
I_Block11
I_C_Block1023
I_Block1023

FIG. 6B

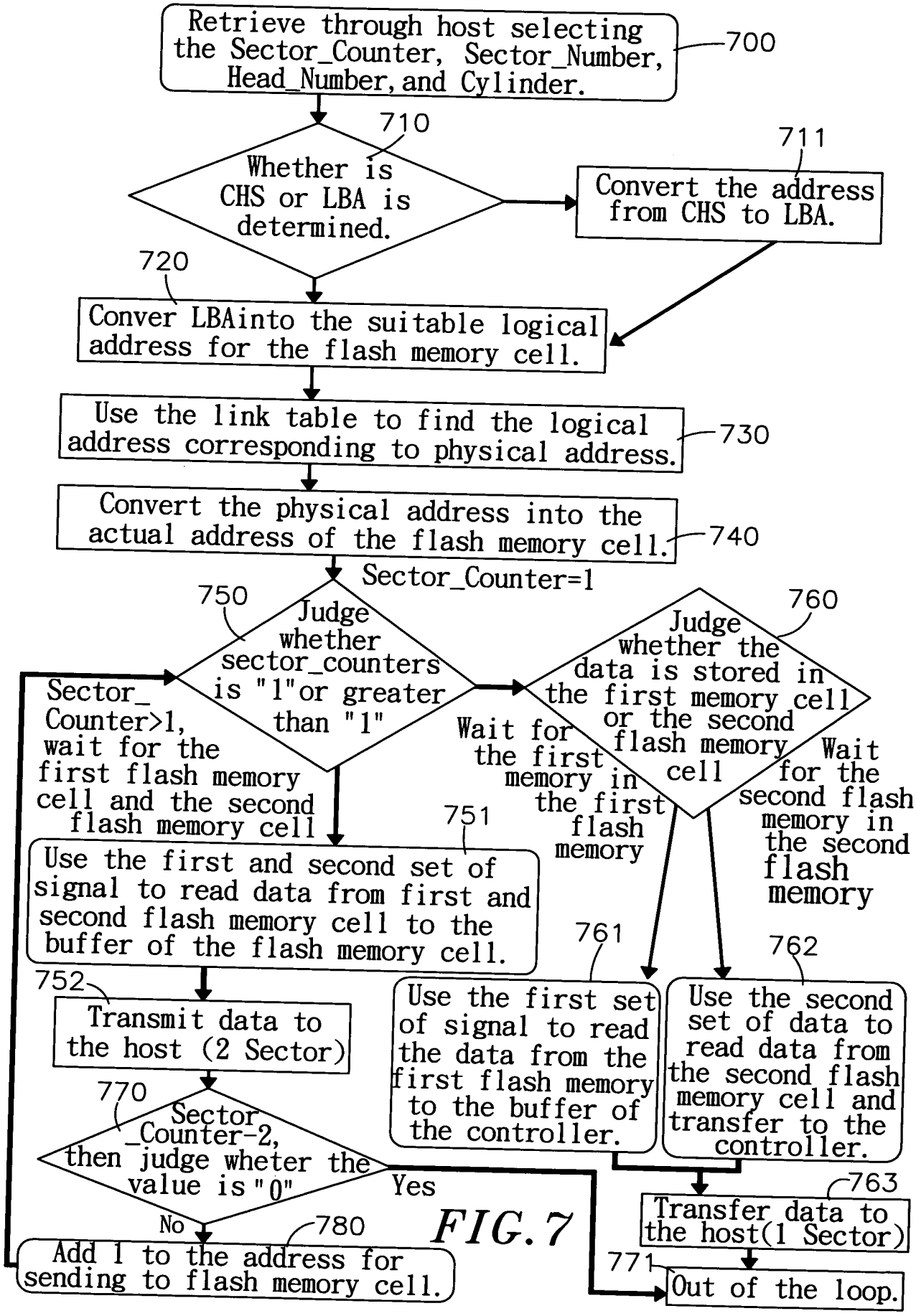

Retrieve through host selecting the Sector_Counter, Sector_Number, Head_Number, and Cylinder.
700
710
Whether is CHS or LBA is determined.
711
Convert the address from CHS to LBA.
720
Conver LBAinto the suitable logical address for the flash memory cell.
Use the link table to find the logical address corresponding to physical address.
730
Convert the physical address into the actual address of the flash memory cell.
740
Sector_Counter=1
750
Judge whether sector_counters is "1"or greater than "1"
760
Judge whether the data is stored in the first memory cell or the second flash memory cell
Sector_ Counter>1, wait for the first flash memory cell and the second flash memory cell
Wait for the first memory in the first flash memory
Wait for the second flash memory in the second flash memory
751
Use the first and second set of signal to read data from first and second flash memory cell to the buffer of the flash memory cell.
761
762
752
Transmit data to the host (2 Sector)
Use the first set of signal to read the data from the first flash memory to the buffer of the controller.
Use the second set of data to read data from the second flash memory cell and transfer to the controller.
770
Sector_Counter-2, then judge wheter the value is "0"
Yes
763
Transfer data to the host(1 Sector)
No
780
Add 1 to the address for sending to flash memory cell.
771
Out of the loop.

FIG. 7

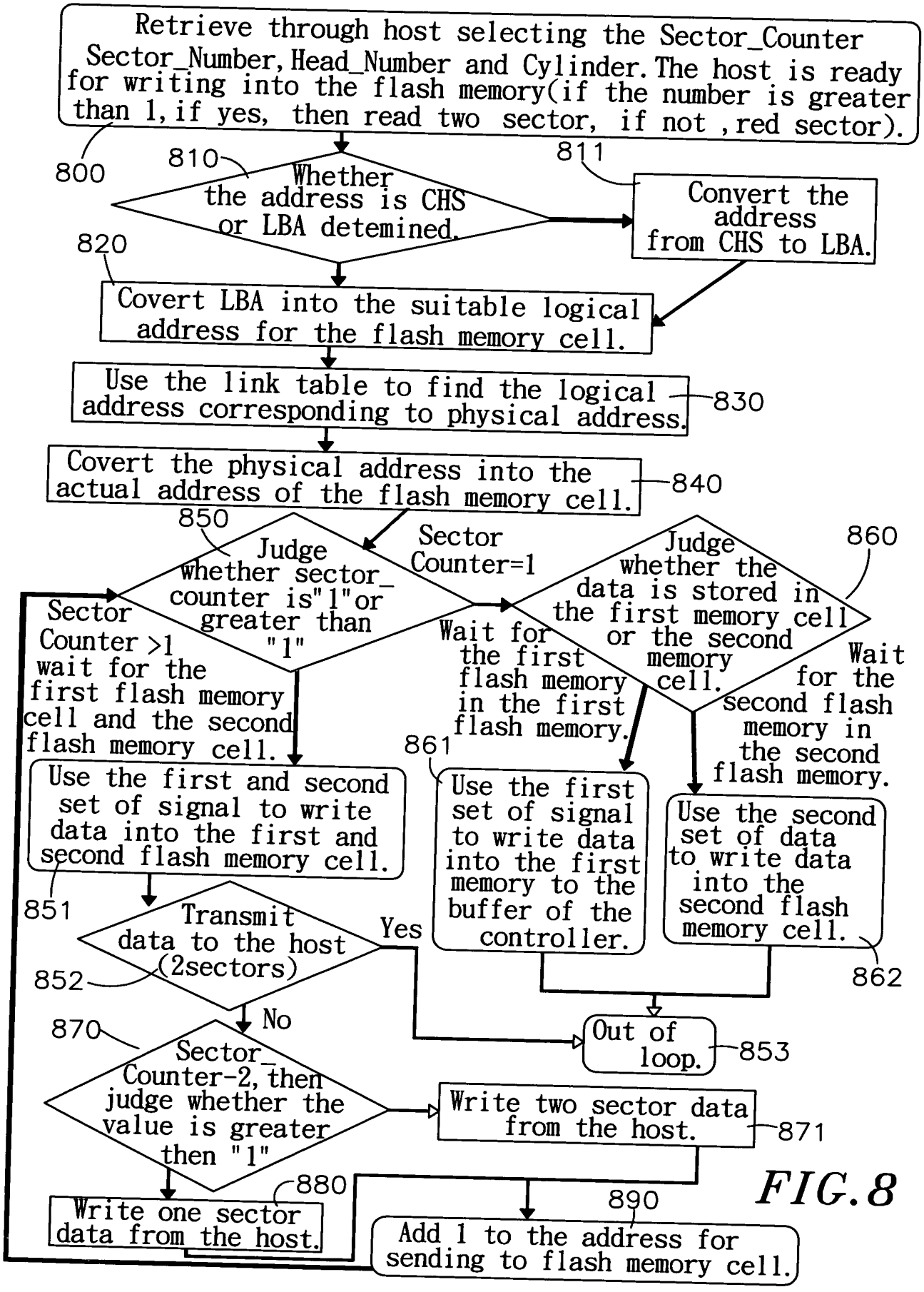

Retrieve through host selecting the Sector_Counter Sector_Number, Head_Number and Cylinder. The host is ready for writing into the flash memory(if the number is greater than 1, if yes, then read two sector, if not , red sector).
800
810
Whether the address is CHS or LBA detemined.
811
Convert the address from CHS to LBA.
820
Covert LBA into the suitable logical address for the flash memory cell.
Use the link table to find the logical address corresponding to physical address.
830
Covert the physical address into the actual address of the flash memory cell.
840
850
Judge whether sector_ counter is"1"or greater than "1"
Sector Counter=1
Sector Counter >1 wait for the first flash memory cell and the second flash memory cell.
860
Judge whether the data is stored in the first memory cell or the second memory cell.
Wait for the first flash memory in the first flash memory.
Wait for the second flash memory in the second flash memory.
861
Use the first and second set of signal to write data into the first and second flash memory cell.
Use the first set of signal to write data into the first memory to the buffer of the controller.
Use the second set of data to write data into the second flash memory cell.
862
851
Transmit data to the host (2sectors)
852
Yes
No
Out of loop.
853
870
Sector_ Counter-2, then judge whether the value is greater then "1"
Write two sector data from the host.
871
880
Write one sector data from the host.
890
Add 1 to the address for sending to flash memory cell.

FIG. 8